

REMARKS

Claim 13 has been rejected under 35 U.S.C. 112, second paragraph for being indefinite. Applicants have amended Claim 13 to replace "the mask layer" with "the silicon nitride layer", thereby providing proper antecedent basis for this element. The rejection of Claim 13 under 35 U.S.C. 112, second paragraph, is thereby overcome.

Claims 1-3 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Nariman et al. (U.S. Patent 6,265,283) in combination with Ghandhi. This rejection is respectfully traversed for the following reasons.

Claim 1 has been amended to recite "patterning a silicon oxynitride layer; then etching a trench in a semiconductor substrate through the patterned silicon oxynitride layer; then conditioning the patterned silicon oxynitride layer, wherein no wet clean step is performed between the etching of the trench and the conditioning of the patterned silicon oxynitride layer; and then performing a wet clean step in the presence of the conditioned silicon oxynitride layer, wherein the wet clean step cleans the trench in the semiconductor substrate. (Emphasis added.)

Support for the first underlined section of Claim 1 is found in the specification as originally filed at paragraph [0022] and in Fig. 3. Support for the second underlined section of Claim 1 is found in the specification as originally filed at paragraph [0024]. Support for the third underlined section of Claim 1 is found in the specification as originally filed at paragraph [0030] and in Fig. 6. No new matter is added. As described in the specification, conditioning the patterned silicon oxynitride layer before

performing a wet clean step prevents the formation of watermarks.

In contrast, Nariman et al. teaches that an isolation trench 42 is formed in substrate 42. (Nariman et al., Col. 5, lines 51-67.) Nariman et al. further teaches that "A wafer clean is then performed using a standard HF dip". (Nariman et al., Col. 6, lines 7-10.) Nariman et al. teaches that a high temperature oxidation process is performed, thereby causing outgassing of the silicon oxynitride layer 46. As the layer 46 outgasses, it densifies and shrinks both vertically and laterally". (Nariman et al., Col. 6, lines 12-19.) Nariman et al. therefore teaches that trench 42 is formed, then a wet clean is performed, and then the silicon oxynitride layer 46 is densified.

Because Nariman et al. teaches that the wet clean step is performed after the trench 42 is formed, and before the silicon oxynitride layer 46 is densified, Nariman et al. fails to teach "no wet clean step is performed between the etching of the trench and the conditioning of the patterned silicon oxynitride layer" as recited by amended Claim 1.

The Examiner indicates that "Ghandhi teaches cleaning surface of semiconductor wafers after each processing step in a fabrication using wet cleaning process." Even if this were true, Ghandhi fails to teach or suggest "no wet clean step is performed between the etching of the trench and the conditioning of the patterned silicon oxynitride layer" as recited by amended Claim 1. In fact, Ghandhi teaches away from this step of amended Claim 1.

For these reasons amended Claim 1 is allowable over Nariman et al. in view of Ghandhi.

Claims 2-4, which depend from Claim 1, are allowable over Nariman et al. in view of Ghandhi for at least the same reasons as Claim 1.

Claims 11-17 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Nariman et al. (U.S. Patent 6,265,283) in combination with Ghandhi, and further in view of Song et al. (U.S. Patent 6,159,823) and Wolf. This rejection is respectfully traversed in view of for the following reasons.

As described above, amended Claim 1 is allowable over Nariman et al. in combination with Ghandhi. Song et al. and Wolf do not overcome the above-described deficiencies of Nariman et al. and Ghandhi. Thus, Claims 11-17, which depend from Claim 1, are allowable for at least the same reasons as Claim 1.

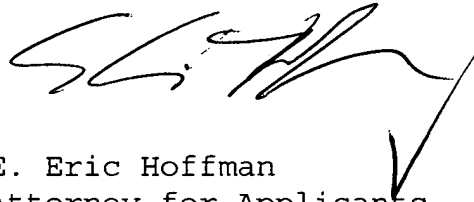
Claims 18-19 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Nariman et al. (U.S. Patent 6,265,283) in combination with Ghandhi, and further in view of Applicant's Admitted Prior Art (AAPA). This rejection is respectfully traversed in view of for the following reasons.

As described above, amended Claim 1 is allowable over Nariman et al. in combination with Ghandhi. AAPA does not overcome the above-described deficiencies of Nariman et al. and Ghandhi. Thus, Claims 18-19, which depend from Claim 1, are allowable for at least the same reasons as Claim 1.

CONCLUSION

Claims 1-4 and 11-19 are pending in the present application. Attached is a document "VERSION WITH MARKINGS TO SHOW CHANGES MADE". Reconsideration and allowance of these claims is respectfully requested. If the Examiner has any questions or comments, he is invited to call the undersigned at (925) 895-3545.

Respectfully submitted,



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Date of Signature

VERSION WITH MARKINGS TO SHOW CHANGES MADECLAIMS

1. (Amended) A method for preventing the formation of watermark defects in a semiconductor process, the method comprising:

patterning a silicon oxynitride layer; then
etching a trench in a semiconductor substrate
through the patterned silicon oxynitride layer; then
conditioning the patterned silicon oxynitride layer, wherein no wet clean step is performed between the etching of the trench and the conditioning of the patterned silicon oxynitride layer; and then

performing a wet clean step in the presence of the conditioned silicon oxynitride layer, wherein the wet clean step cleans the trench in the semiconductor substrate.

13. (Amended) The method of Claim 12, further comprising etching the silicon oxynitride layer, the silicon nitride [mask] layer, the pad oxide and the semiconductor substrate through the photoresist mask, thereby forming the [a] trench in the semiconductor substrate.